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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,118	04/01/2004	Ramadas Lakshmikanth Pai	15483US02	8484

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EXAMINER	
HOLDER, ANNER N	

ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
04/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,118	PAI ET AL.	
	Examiner	Art Unit	
	ANNER HOLDER	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/28/09*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7-9 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5, 7-9, and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/01/04; 09/14/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 01/28/09 have been fully considered but they are not persuasive. As to Applicant's arguments Examiner respectfully disagrees. Yoshioka reference was not cited by the Examiner as teaching "fetch reference pixels for a first portion of a picture" and "loads the memory controller with second portion while the memory controller fetched the reference pixels". Ran teaches a memory is divided into several parts for processing and for loading reference pixels while processing is being performed. [col. 3 lines 4-10] The simultaneous processing or writing with the loading or reading of reference values as taught in Ran is being used in combination with the media processing device of Yoshioka et al. which fairly suggest and reads upon the language of claims 1 and 5. It is well known in the art that memory is capable of performing simultaneous read/write operations as further evidenced Bellini et al. US 6,950,337 B2, Kadota US 4,447,891, Kootstra US 6,880,056 B2. The use of simultaneous reading and writing to and from a memory device has known advantages such as improving processing efficiency, the use of the known techniques would have been a predictable modification, and one of ordinary skill in the art would recognize that it would improve similar devices in the same way. Although Ran is directed toward encoding it would have been obvious to one of ordinary skill in the art that the technique discussed above is applicable to decoding, as decoding is a mirror process of encoding.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 7-9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (Yoshioka) US 6,310,921 B1 in view of Ran et al. (Ran) US 5,706,059.

4. As to claim 1, Yoshioka teaches a video request manager [Fig. 3; Fig. 4; Fig. 16] comprising: a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; [Fig. 4; Fig. 16; Col. 11 Line 64 – Col. 12 Line 7; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14] and a second state machine for commanding a memory controller to write a second portion of the picture, [Fig. 4; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14, 20-27] memory controller fetches the reference pixels. [Col. 14 Lines 38-45]

Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem.

However, Yoshioka is silent as to the second state machine loads the memory controller with the second portion while the memory controller fetches as claimed.

Ran teaches the second state machine loads the memory controller with the second portion while the memory controller fetches. [abstract; col. 3 lines 4-10]

It would have been obvious at the time the invention was made to incorporate the simultaneous read/search and write teachings of Ran with the device of Yoshioka allowing for efficiency in image coding.

5. As to claim 2, Yoshioka (modified Ran) teaches the second state machine commands the memory controller to write the second portion, such that a resource contention occurs between the command to fetch reference pixels, and the command to write the second portion. [Yoshioka - Fig. 3; Fig. 4]

6. As to claim 3, Yoshioka (modified Ran) teaches the second state machine commands the memory controller to write the second portion, such that the command to fetch reference pixels is given priority during the resource contention. [Yoshioka - Col. 11 Lines 39-41; Col. 14 Lines 38-45]

7. As to claim 5, Yoshioka teaches a circuit for decoding video data, [Fig. 4 (1002); Col. 11 Lines 30-41; Col. 12 Line 62 – Col. 13 Line 4] said circuit comprising: a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture; [Col. 5 Lines 62-64; Col. 5 Line 67 Col. 6 Line 2; Fig. 6; Col. 14 Lines 38-45; Col. 13 Lines 66-67; Fig. 10; Col. 18 Lines 9-14; Fig. 21 Fig. 19; Col. 16 Lines 26-54] a motion compensator for decoding another portion of the picture; [Col. 15 Line 65 – Col. 16 Line 2; Fig. 15 (A&B); Col. 23 Lines 62-67] and a video request manager comprising: a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; [Fig. 4; Fig. 16; Col. 11 Line 64 – Col. 12 Line 7; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14] and a second state

machine for issuing a command to write a second portion of the picture. [Fig. 4; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14, 20-27] a memory controller fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command. [Col. 15 Line 65 –Col. 16 Line 2; Fig. 15 (A&B); Col. 23 Lines 62-67]

Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem. However, Yoshioka is silent as to memory controller loads the second portion of the picture while fetching as claimed.

Ran teaches the memory controller loads the second portion of the picture while fetching. [abstract; col. 3 lines 4-10]

It would have been obvious at the time the invention was made to incorporate the simultaneous read/search and write teachings of Ran with the device of Yoshioka allowing for efficiency in image coding.

8. As to claim 7, Yoshioka (modified Ran) teaches the memory controller [Fig. 4 (6); Fig. 16 (26)] further comprises: an arbiter for causing the memory controller to give priority to the command to fetch the reference pixels. [Yoshioka - Col. 11 Lines 39-41; Col. 14 Lines 38-45]

9. As to claim 8, Yoshioka (modified Ran) teaches the memory controller [Fig. 4 (6); Fig. 16 (26)] further comprises: a write buffer for storing the second portion of the

picture while fetching the reference pixels. [Yoshioka - Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14]

10. As to claim 9, Yoshioka (modified Ran) teaches the memory controller [Fig. 4 (6); Fig. 16 (26)] writes the second portion of the picture from the write buffer to a memory system, after fetching the reference pixels. [Yoshioka - Col. 11 Lines 39-41; Col. 14 Lines 38-45]

11. As to claim 15, Yoshioka (modified Ran) teaches the second state machine loads the memory controller with the second portion reconstructed from decoding while the memory controller fetches the reference pixels. [Ran - abstract; col. 3 lines 4-10]

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Hoogenboom et al. US 5,675,387; Bellini et al. US 6,950,337 B2; Kadota US 4,447,891; Kootstra US 6,880,056 B2.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANNER HOLDER whose telephone number is (571)270-1549. The examiner can normally be reached on M-Th, M-F 8 am - 3 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anner Holder/
Examiner, Art Unit 2621

/Tung Vo/
Primary Examiner, Art Unit 2621